HIGH VOLTAGE SERIES

JARO high voltage series Multilayer Ceramic Capacitors are constructed by depositing alternative layers of ceramic dielectric materials and internal metallic electrodes, by using advanced ceramic manufacturing technology, and co-firing into an indestructible homogeneous body, then completed with application of metal end terminations which are fired on to assure that permanent connection of individual internal electrodes are in parallel.

The terminations are nickel-plated and then solder plated to give the chip capacitors nickel-barrier terminations which have much better leaching resistance during soldering.

Reliable performances are built-in through exact formulation of dielectric powders, preparation of conductive paste, advanced automatic manufacturing, and strict quality control to assure excellent control in dielectric thickness, electrode integrity, and electrode-to-termination continuity.

JARO offers the high performance MLCC of high voltage. There are five standard sizes 0805, 1206, 1210, 1808, and 1812 and ranging from 100V to 2KV in COG and X7R characteristics.

RECOMMENDED APPLICATIONS

Modems

LAN/WAN Interface

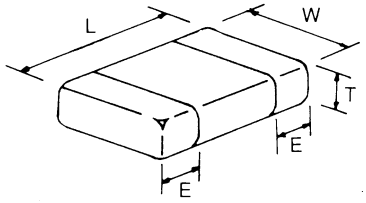
Power Supplies

Telecom Devices

Industrial Controls

MECHANICAL DATA

Component outline:



CAPACITOR DIMENSIONS

Size		0805	1206	1210	1808	1812	
(L) Length	mm (in)	2.00 ± 0.20 (.080 ± .008)	3.20 ± 0.20 (.126 ± .008)	3.20 ± 0.30 (.126 ± .012)	4.50 ± 0.30 (.177 ± .012)	4.50 ± 0.30 (.177 ± .012)	
(W) Width	mm (in)	1.20 ± 0.20 (.050 ± .008)	1.60 ± 0.20 (.063 ± .008)	2.50 ± 0.30 (.100 ± .012)	2.00 ± 0.20 (.080 ± .008)	3.20 ± 0.30 (.126 ± .012)	
(E) Termination	mm (in)	0.50 ± 0.20 (.020 ± .008)	0.50 ± 0.20 (.020 ± .008)	0.50 ± 0.20 (.020 ± .008)	0.64 ± 0.38 (.025 ± .015)	0.64 ± 0.38 (.025 ± .015)	

Dimensions are in millimeters, dimensions in parenthesis are in inches.

CAPACITANCE RANGE: COG

EIA	COG																							
Cap	250V				500V			1.0KV				1.5KV				2.0KV				3.0KV			
(pF)	0805	1206	1210	1812	1206	1210	1812	1206	1210	1808	1812	1206	1210	1808	1812	1206	1210	1808	1812	1206	1210	1808	1812
10																							
12																							
15																							
18																							
22																							
27																							
33																							
39																							
47																							
56																							
68																							
82																							
100																							
120																							
150																							
180																							
220																							
270																							
330																							
390																							
470																							
560																							
680																							
820																							
1000																							
1200																							
1500																							
1800																							
2200																							
2700																							
3300																							
3900																							
4700																							
5600																							
6800																							
8200																							
10000																							

Other capacitance values and voltages are available upon request.

The thickness of chip capacitors might be changed due to the improvement of the production technology.

CAPACITANCE RANGE: X7R

EIA	X7R																		
Cap	100V				250V				500V			1.0KV				2.0KV			
(pF)	0805	1206	1210	1812	0805	1206	1210	1812	1206	1210	1812	1206	1210	1808	1812	1206	1210	1808	1812
100												■				■			
120												■				■			
150												■				■			
180												■				■			
220												■				■			
270												■				■			
330												■				■			
390												■				■			
470												■				■			
560												■				■			
680												■				■			
820												■				■			
1000	■	■			■	■			■			■	■	■	■	■	■	■	■
1200	■	■			■	■			■			■	■	■	■		■	■	■
1500	■	■			■	■			■			■	■	■	■		■	■	■
1800	■	■			■	■			■			■	■	■	■		■	■	■
2200	■	■			■	■			■			■	■	■	■				■
2700	■	■			■	■			■	■			■	■	■				■
3300	■	■			■	■			■	■			■	■	■				■
3900	■	■			■	■			■	■			■	■	■				
4700	■	■			■	■			■	■	■				■				
5600	■	■			■	■				■	■				■				
6800	■	■			■	■				■	■				■				
8200	■	■			■	■				■	■				■				
10000	■	■				■					■								
12000	■	■				■					■								
15000		■				■					■								
18000		■				■					■								
22000		■				■	■				■								
27000		■					■												
33000		■					■												
39000		■					■												
47000		■	■				■	■											
56000		■	■					■											
68000		■	■					■											
82000		■	■					■											
100000		■	■	■				■											
120000			■	■															
150000				■															
180000				■															
220000				■															

Other capacitance values and voltages are available upon request.

The thickness of chip capacitors might be changed due to the improvement of the production technology.

ELECTRICAL SPECIFICATIONS

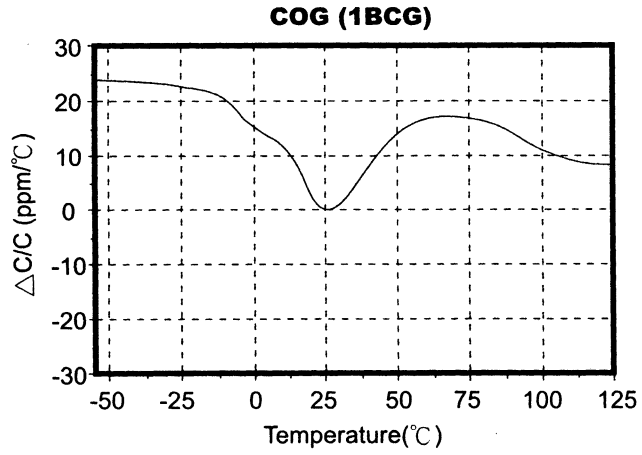
Dielectric Code	EIA	COG	X7R
	IEC	1BCG	2R1
Temperature Characteristics	*1	0±30ppm/°C, C>20PF 0^{+120}_{-40} ppm/°C, C≤20PF	ΔC±15% maximum over -55°C to +125°C
Operating Temperature Range		-55°C to +125°C	-55°C to +125°C
Measuring Conditions for Capacitance and D.F.	*2	1 MHz, 1 Vrms, C≤1000PF 1 KHz, 1 Vrms, C>1000PF	1 KHz, 1 Vrms
Dissipation Factor (D.F.) and Tangent of Loss Angle (tan δ)		≤0.1% for C≥30PF ≤100%/(400+20C) for C<30PF	rated voltage ≤2.5% ≥50V ≤3.5% 25V 16V ≤5.0% 10V 6.3V
Insulation Resistance (I.R.) after 60 secs. charging at rated voltage, 25°C, 55% RH max.		≥100 Gohms or ≥1,000 MΩ • μF whichever is less	≥100 Gohms or ≥1,000 MΩ • μF whichever is less
Voltage Proof, 25°, 1-5 secs.		2.5 x Rated Voltage	2.5 x Rated Voltage
Capacitance Aging		0	≈ 1.5% per decade hour

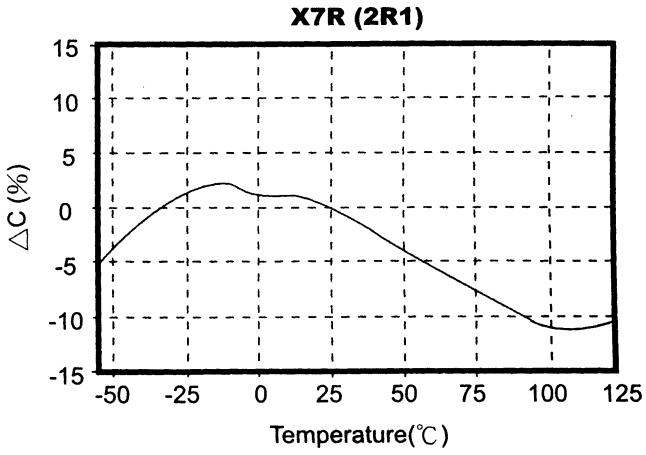
*1. Class I (COG) capacitors shall be conditioned for 96 ± 4hr by heating in a circulationg air oven at a temperature of 55 ± 2°C and a relative humidity not exceeding 20%. The capacitor shall then be allowed to cool in a desiccator using a suitable desiccant, such as activated alumina or sillica gel, and shall be kept therein from the time of removal from the oven to the beginning of the specified tests.

Class II (X7R, Z5U, Y5V) capacitors shall be made a special pre-conditioning before a test or a sequence of tests under the following conditions: Exposure at 150 ± 10°C for 1 hr, followed by setting the capacitor at room temperature for 24 ± 1 hr.

*2. Capacitance is within specified tolerance; measured 1000 hours after date of manufacture because of capacitance aging of class II capacitor.

TYPICAL PERFORMANCE CURVES





ENVIRONMENTAL SPECIFICATIONS

Test	Test Conditions	Post-Test Inspection Requirements
Solderability	**IEC 384-10 4.11 /JIS C 5102 8.13** Solder 60 Sn/40 Pb, 235 ± 5°C Immersed for 5 secs.	At least 75% of termination area should be well tinned. No visible damage.
Resistance to Soldering Heat *1	**IEC 384-10 4.10 /JIS C 5102 8.14** Immersed in solder bath at 260 ± 5°C for 10 ± 1 secs. Recovery: 6~24 hrs. (COG) 24 ± 2 hrs. (X7R)	At least 75% of termination should be covered by solder. No visible damage. **ΔC/C**: **COG (1BCG)** ≤ ± 0.5%, or ± 0.5pF whichever is greater; **X7R (2R1)** ≤ +10% -5%
Rapid Change of Temperature *2	**IEC 384-10 4.12 /JIS C 5102 9.3** -55C to +125°C, 5 cycles (COG, X7R) Duration: 30 mins. Recovery: 6~24 hrs. (COG) 24 ± 2 hrs. (X7R)	No visible damage. **ΔC/C**: **COG (1BCG)** ≤ ± 1%, or ± 1pF whichever is greater; **X7R (2R1)** ≤ +10% **D.F.**: ≤ 1.5 x initial requirement **I.R.**: ≥ 0.25 x initial requirement
Endurance (Life Test) *3	**IEC 384-10 4.15** 1000 hrs. at maximum temperature applied with 2.0 x U_R (≤ 250V), 1.5 x U_R (≤ 1KV), 1.2 x U_R (≤ 2KV) Recovery: 6~24 hrs. (COG) 24 ± 2 hrs. (X7R)	No visible damage. **ΔC/C**: **COG (1BCG)** ≤ ± 2%, or ± 1pF whichever is greater; **X7R (2R1)** ≤ +20% **D.F.**: **COG (1BCG)** ≤ 2.0 x initial requirement; **X7R (2R1)** ≤ 1.5 x initial requirement **I.R.**: ≥ 0.25 x initial requirement
Humidity Test (Damp heat, steady state) *4	**IEC 384-10 4.14 /JIS C 5102 9.5** 500 hrs. at 40 ± 2°C, 90-95% RH Recovery: 6~24 hrs. (COG) 24 ± 2 hrs. (X7R)	No visible damage. **ΔC/C**: **COG (1BCG)** ≤ ± 2%, or ± 1pF whichever is greater; **X7R (2R1)** ≤ +10% **D.F.**: **COG (1BCG)** ≤ 2.0 x initial requirement; **X7R (2R1)** ≤ 1.5 x initial requirement **I.R.**: ≥ 0.25 x initial requirement
Adhesion	**IEC 384-10 4.8 /JIS C 5102 8.11.2** Capacitors mounted on a substrate, a force of 5N applied perpendicular to the plane of substrate and parallel the line joining the centre of terminations for 10 ± 1 secs.	No visible damage.

*1~4: Class II (X7R, Z5U, Y5V) capacitors shall be made a special pre-conditioning before a test or a sequence of tests under the following conditions: Exposure at 150 ± 10°C for 1 hr, followed by setting the capacitor at room temperature for 24 ± 1 hr.

PACKAGING

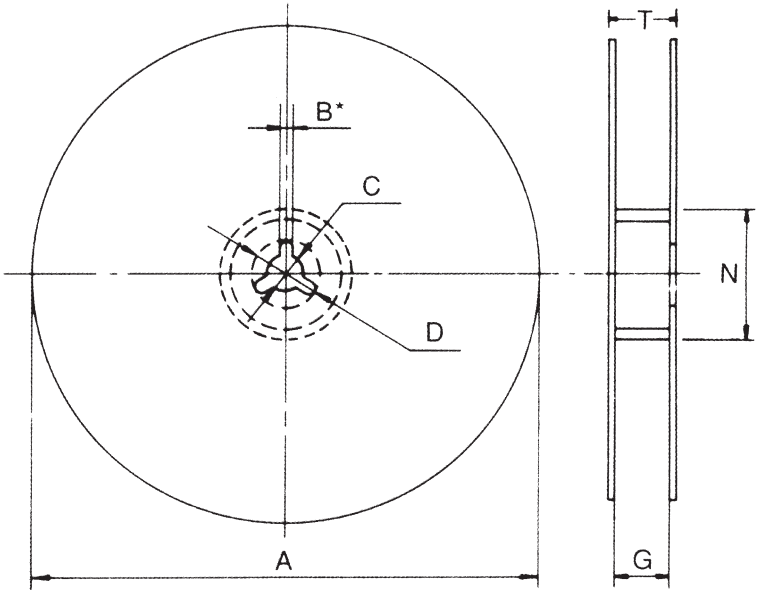
BULK PACKAGE

All JARO Multilayer Ceramic Chip Capacitors are available in sealed plastic bag. The number of chips per bag depends on size and thickness of chip capacitors.

TAPE AND REEL PACKAGE

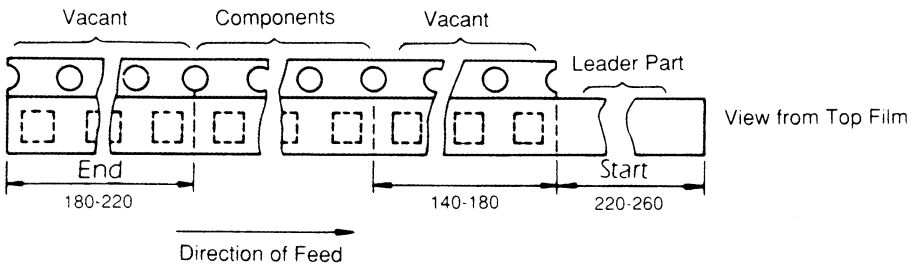
Taping is in accordance with EIA RS-481 or IEC 286-3

REEL FOR TAPING



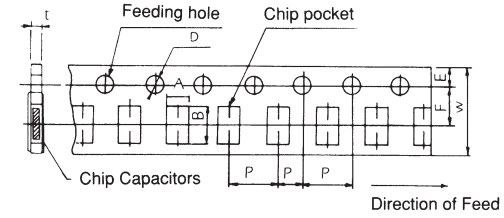
Unit: mm

Symbol	A	N	C	D	B	G	T	
Dimension	178±2.0 178±2.0	50 min. 50 min.	130±0.5 130±0.5	20 min. 20 min.	2.0±0.5 2.0±0.5	10.0±1.5 13.8±1.5	14.9 max. 16.7 max.	



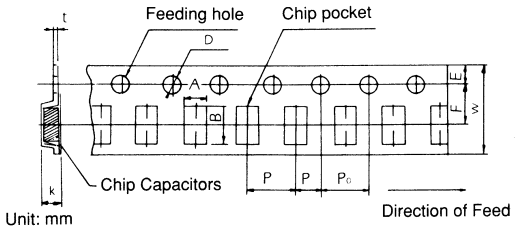
Unit: mm

CARDBOARD TAPE DIMENSIONS



Unit: mm

EMBOSSED TAPE DIMENSIONS



Unit: mm

CARDBOARD TAPE

Unit: mm

Symbol / Size Code	A	B	W	F	E	P_1	P_2	P_0	ØD	t_1
0402	0.65	1.15	8.0 ±0.3	3.5 ±0.06	1.75 ±0.1	2.0 ±0.05	2.0 ±0.05	4.0 ±0.1	1.5 +0.1 –0	1.1 max.
0603	1.25 ±0.2	2.05 ±0.2	8.0 ±0.2	3.5 ±0.05		4.0 ±0.1				
0805	1.65 ±0.2	2.4 ±0.2								
1206	2.0 ±0.2	3.6 ±0.2								

EMBOSSED TAPE

Unit: mm

Symbol / Size Code	A	B	W	F	E	P_1	P_2	P_0	ØD	t_1	K
0805	1.6 ±0.2	2.4 ±0.2	8.0 ±0.2	3.5 ±0.05	1.75 ±0.1	4.0 ±0.1	2.0 ±0.05	4.0 ±0.1	1.5 +0.1 –0	0.3 max.	2.0 max.
1206	1.95 ±0.2	3.6 ±0.2									
1210	2.8 ±0.2	3.7 ±0.2									
1808	2.4 ±0.2	4.9 ±0.2	1.2 ±0.2	5.5 ±0.05	1.75 ±0.1	8.0 ±0.1	2.0 ±0.1	8.0 ±0.1	1.5 +0.1-0	0.3 max.	2.5 max.
1812	3.6 ±0.2	4.9 ±0.2	1.2 ±0.3	5.5 ±0.1	1.75 ±0.1	8.0 ±0.1	2.0 ±0.1	8.0 ±0.1	1.5 +0.1-0	0.3 max.	2.5 max.

STANDARD PACKING QUANTITY PER REEL

Chip Size	Chip Thickness, max.	Cardboard Tape	Embossed Tape
0402	0.55 mm	10,000	10,000
0603	0.95 mm	4,000	–
0805	0.95 mm	4,000	–
	1.25 mm	–	2,000
1206	0.95 mm	4,000	4,000
	1.25 mm	–	2,000
1210	1.30 mm	–	3,000
1808	1.30 mm	–	3,000
	1.60 mm	–	2,000
1812	1.30 mm	–	1,500
	1.60 mm	–	1,000

APPLICATION NOTES

STORAGE

To prevent the damage of solderability of terminations, the following storage conditions are recommended:

- Ambient temperature less than 40°C.
- Relative humidity less than 70% RH.
- No harmful gases containing sulfur or chlorine.

In the case of bulk packaging do not unpack the minimum package. In case of unpacking, seal again or store in a desiccator containing drying agent.

HANDLING

Chip Capacitors should be handled with care to avoid contaminatin or damage. The use of vacuum pick-up or plastic tweezers is recommended for manual placement. Tape and reeled packages are suitable for automatic pick and placement machine.

PREHEAT

In order to minimize the risk of thermal shock during soldering, a carefully controlled preheat is required. The rate of preheat should not exceed 4°C per second and the final preheat temperature should be within 100°C of the soldering temperature for small chips such as 0603, 0805 and 1206, within 50°C of the soldering temperature for bigger chips such as 1210 and 1812, etc.

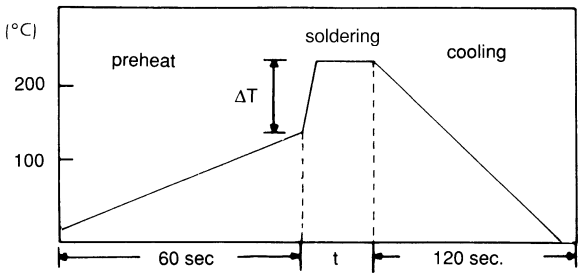
SOLDERING

Use mildly activated rosin RA and RMA fluxes, do not use acivated flux. The amount of solder in each solder joint should be controlled to prevent the damage of chip capacitors caused by the stress between solder, chips, and substrate.

Hand soldering with temperature-controlled iron not exceeding 30 watts and diameteter of tip less than 1.2 mm is recommended, tip of iron should not contact the ceramic body directly, and the temperature of iron should be set to not more than 260°C.

For bigger chips such as 1210, 1808 and 1812, etc. wave soldering and hand soldering are not recommended.

Recommended soldering profiles as following:



Soldering	Solder Temp. (T)	Soldering Time (t)
Reflow	220-240°C	<15 sec.
Wave	230-250°C	<5 sec.

Chip Size	ΔT
0402, 0603, 0805, 1206	100°C
1210, 1808, 1812	50°C

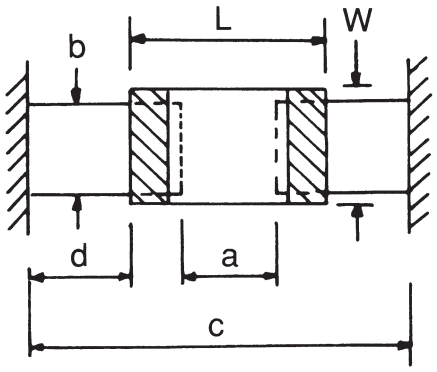
COOLING

After soldering, cool the chips and the substrate gradually to room temperature. Natural cooling in air is recommended to minimize stress in the solder joint. A cooling rate not exceeding 4°C per second should be used when forced cooling is necessary.

CLEANING

All flux residue must be removed by using suitable electronic-grade vapor-cleaning solvents to eliminate contaminations that could cause electrolytic surface corrosion. Good results can be obtained by using ultrasonic cleaning of the solvent. The choice of the proper system is dependent upon many factors such as component mix, flux, solder paste and assembly method. The ability of the cleaning system to remove flux residues and contamination from under the chips is very important.

RECOMMENDED PAD DIMENSIONS



Unit: mm (inches)

Chip Size	L	W	a	b	c	d	
0402	1.0 (.039)	0.5 (.02)	0.6 (.023)	0.6 (.023)	1.7 (.067)	0.35 (.014)	
0603	1.6 (.063)	0.8 (.032)	0.7 (.028)	0.7 (.028)	2.1 (.083)	0.7 (.028)	
0805	2.0 (.080)	1.2 (.050)	1.0 (.040)	1.0 (.040)	2.6 (.102)	0.8 (.032)	
1206	3.2 (.126)	1.6 (.063)	2.2 (.087)	1.4 (.055)	4.4 (.173)	1.1 (.043)	
1210	3.2 (.126)	2.5 (.100)	2.2 (.087)	2.2 (.087)	4.4 (.173)	1.1 (.043)	
1808	4.5 (.177)	2.0 (.080)	3.5 (.137)	2.8 (.110)	6.7 (.264)	1.1 (.043)	
1812	4.5 (.177)	3.2 (.126)	3.5 (.137)	2.8 (.110)	6.7 (.264)	1.1 (.043)	